


PAGE	TITLE
------	-------

[illegible]

			
Title			
<b>COVER SHEET</b>			
Size	Document Number	GA-F2A88XM-D3H	Rev
Custom			3.1
Date: Friday, September 26, 2014		Sheet 1 of 29	

**Model Name:GA-F2A88XM-D3H**

### Component value change history

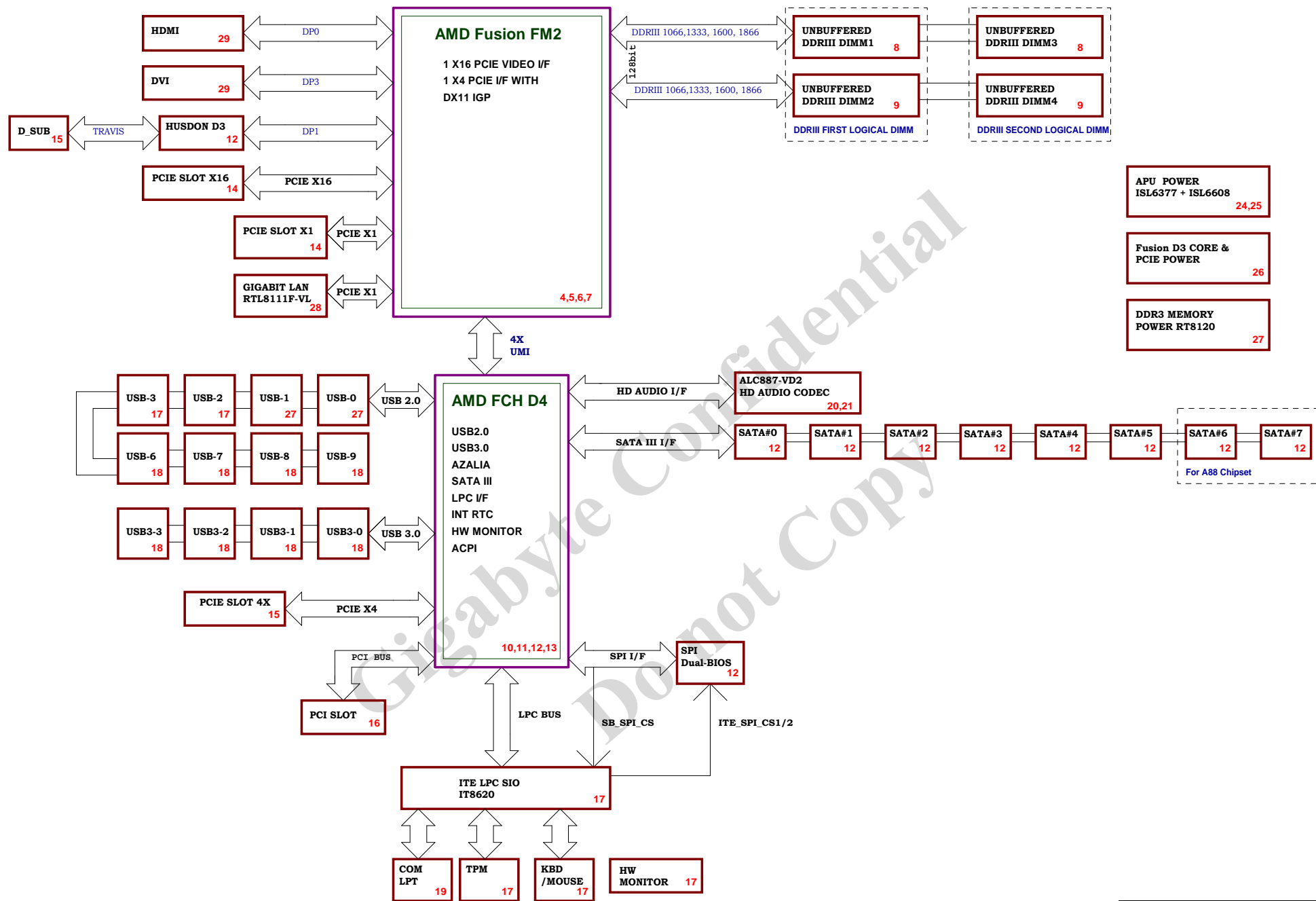
**Version: 3.1**

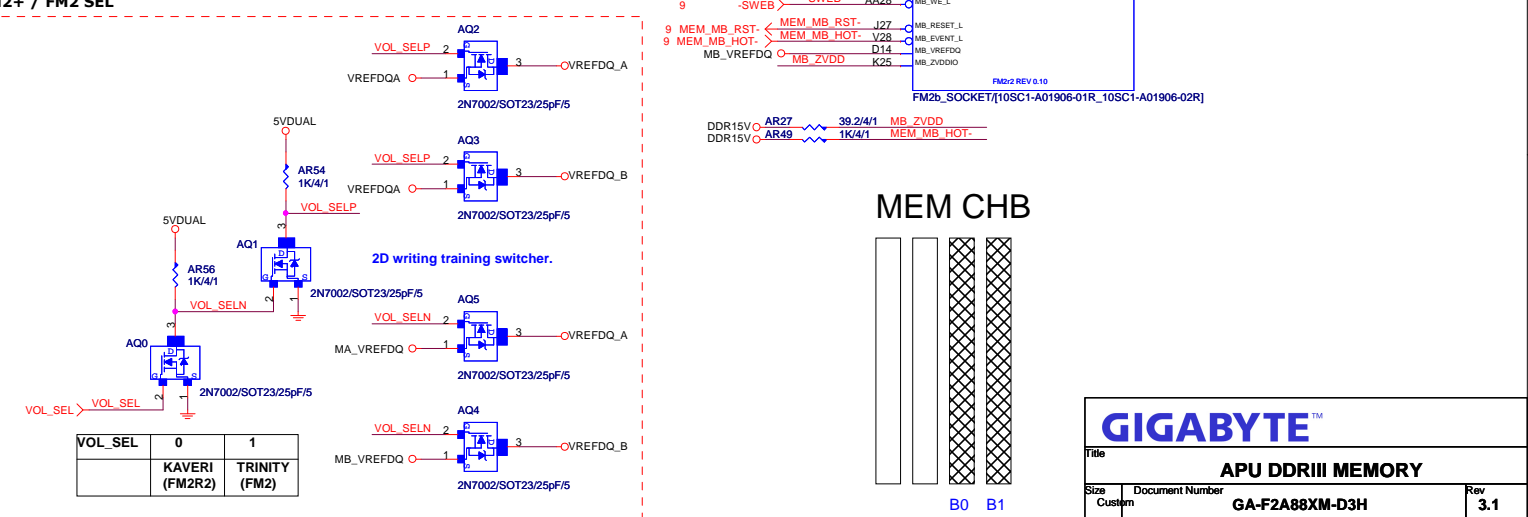
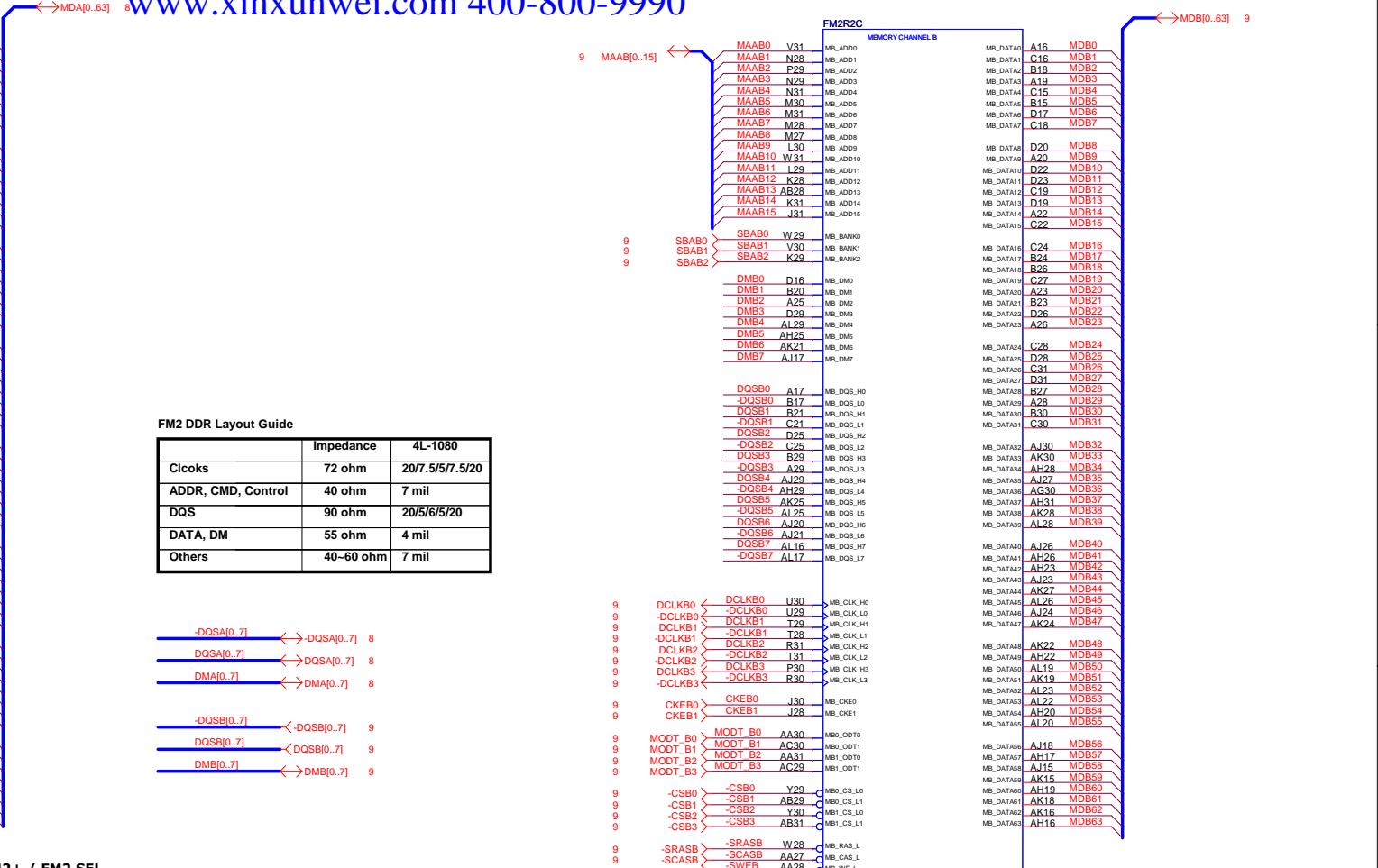
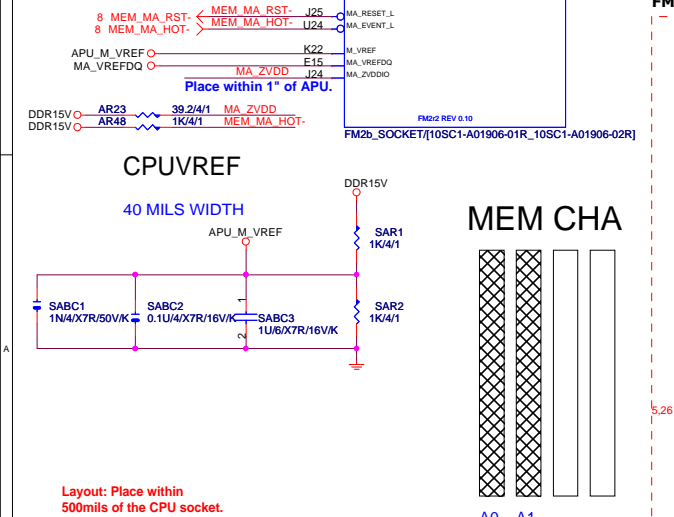
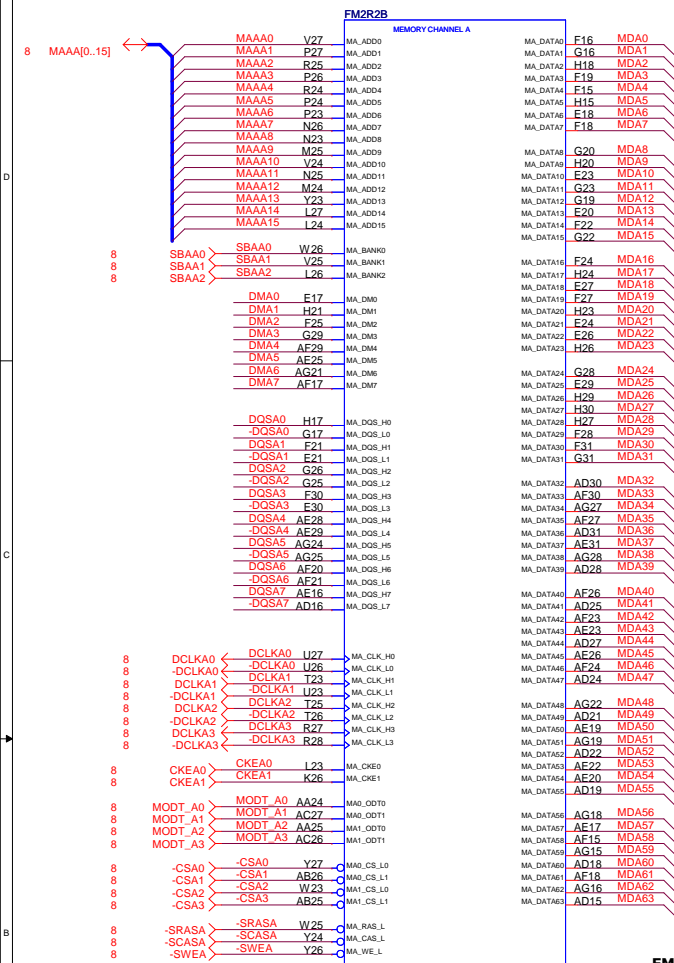
**P-Code: U12061-0**

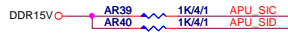
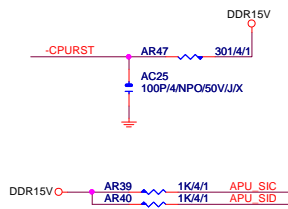
[illegible]

### Circuit or PCB layout change for next version

[illegible]





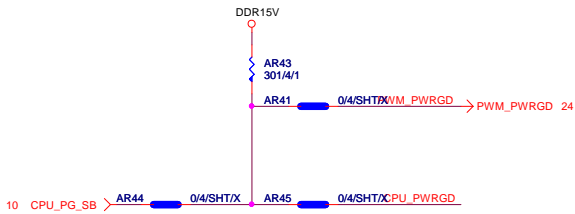


FM2 CPU Clock Layout Guide

	Impedance	4L-1080
APU Clock	85 ohm	20/4.5/7.5/4.5/20
DISP Clcok	85 ohm	20/4.5/7.5/4.5/20
DP TX/RX	85 ohm	20/4.5/7.5/4.5/20
	55 ohm	4 mil
	40~60 ohm	7 mil

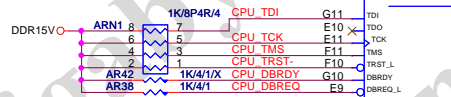
APU Spread 100Mhz clock

DP Non-Spread 100Mhz clock

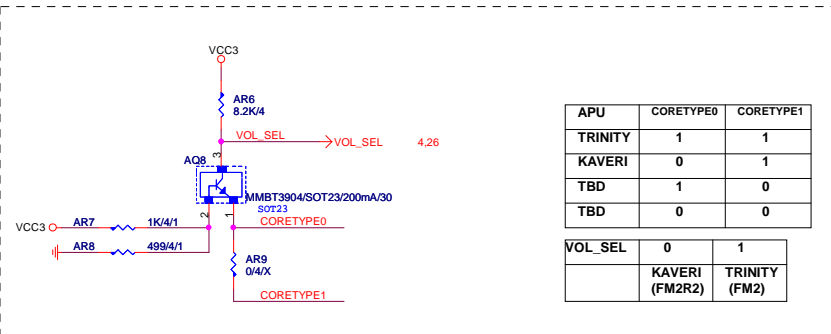


APU Spread 100Mhz clock

DP Non-Spread 100Mhz clock



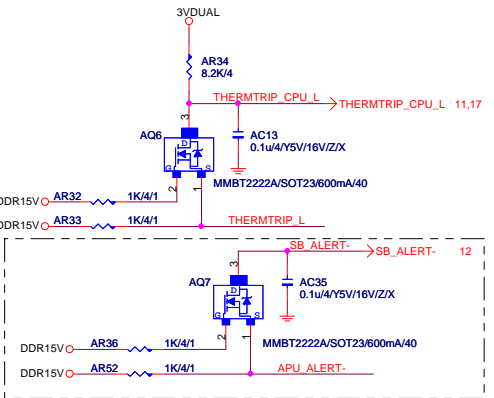
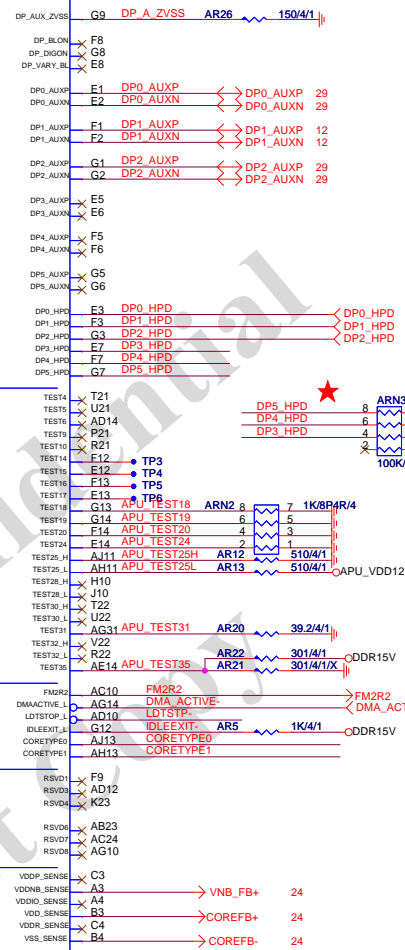
FM2+ / FM2 SEL



Group	APU FM2
Group A	VDDA25:1.8~2.7V/0.5A
Group A	DDR15V:0.8~2.3V/30A
Group B	VCORE: 0.8~2.0V/120A
Group B	VCORE_NB:1.2V/50A
Group B	VDDP:1.2V/5A
Group B	VDDR:1.2V/5A

Gropu A must early than Group B

Placed within 1500 mils from APU



TEST35: high=&gt;HDMI enable, low=&gt;HDMI disable.

FM2R2 AR31 8.2K/4/1 3VDUAL

DMA\_ACTIVE- AR30 1K/4/1 3VDUAL

LDTSTP- AR53 1K/4/1X 3VDUAL

Hudson DG\_1.80

APU	CORETYPE0	CORETYPE1
TRINITY	1	1
KAVERI	0	1
TBD	1	0
TBD	0	0

VOL_SEL	0	1
	KAVERI (FM2R2)	TRINITY (FM2)

GIGABYTE™

Title	Document Number	Rev
APU CONTROL	GA-F2A88XM-D3H	3.1
Size	Custom	
Date	Wednesday, September 24, 2014	Sheet 5 of 29

FM2R2A

PCIEXPRESS

GRAPHICS

GPP

UMI

FM2b REV 1.0

FM2b\_SOCKET[10SC1-A01906-01R\_10SC1-A01906-02R]

P\_GFX\_TXP0 AC2 EXP A TXP0  
P\_GFX\_TXN0 AC1 EXP A TXN0  
P\_GFX\_TXP1 AC4 EXP A TXP1  
P\_GFX\_TXN1 AC5 EXP A TXN1  
P\_GFX\_TXP2 AB2 EXP A TXP2  
P\_GFX\_TXN2 AB3 EXP A TXN2  
P\_GFX\_TXP3 AA2 EXP A TXP3  
P\_GFX\_TXN3 AA1 EXP A TXN3  
P\_GFX\_TXP4 AA4 EXP A TXP4  
P\_GFX\_TXN4 AA5 EXP A TXN4  
P\_GFX\_TXP5 Y2 EXP A TXP5  
P\_GFX\_TXN5 Y3 EXP A TXN5  
P\_GFX\_TXP6 W2 EXP A TXP6  
P\_GFX\_TXN6 W1 EXP A TXN6  
P\_GFX\_TXP7 W4 EXP A TXP7  
P\_GFX\_TXN7 W5 EXP A TXN7  
P\_GFX\_TXP8 V2 EXP A TXP8  
P\_GFX\_TXN8 V3 EXP A TXN8  
P\_GFX\_TXP9 U2 EXP A TXP9  
P\_GFX\_TXN9 U1 EXP A TXN9  
P\_GFX\_TXP10 U4 EXP A TXP10  
P\_GFX\_TXN10 U5 EXP A TXN10  
P\_GFX\_TXP11 T2 EXP A TXP11  
P\_GFX\_TXN11 T3 EXP A TXN11  
P\_GFX\_TXP12 R2 EXP A TXP12  
P\_GFX\_TXN12 R1 EXP A TXN12  
P\_GFX\_TXP13 R4 EXP A TXP13  
P\_GFX\_TXN13 R5 EXP A TXN13  
P\_GFX\_TXP14 P2 EXP A TXP14  
P\_GFX\_TXN14 P3 EXP A TXN14  
P\_GFX\_TXP15 N2 EXP A TXP15  
P\_GFX\_TXN15 N1 EXP A TXN15

TX CAP close to CPU side

P\_GPP\_TXP0 AF2 GPP TXP0 AC33  
P\_GPP\_TXN0 AF3 GPP TXN0 AC34  
P\_GPP\_TXP1 AE2 PCIE1\_OP  
P\_GPP\_TXN1 AE1 PCIE1\_ON  
P\_GPP\_TXP2 AE4  
P\_GPP\_TXN2 AE5  
P\_GPP\_TXP3 AD2  
P\_GPP\_TXN3 AD3

P\_UMI\_TXP0 AJ5 A TX0P C AC1  
P\_UMI\_TXN0 AJ4 A TX0N C AC2  
P\_UMI\_TXP1 AH3 A TX1P C AC3  
P\_UMI\_TXN1 AH2 A TX1N C AC4  
P\_UMI\_TXP2 AG1 A TX2P C AC5  
P\_UMI\_TXN2 AG2 A TX2N C AC6  
P\_UMI\_TXP3 AG5 A TX3P C AC7  
P\_UMI\_TXN3 AG4 A TX3N C AC8

P\_ZVDDP AJ1 P\_ZVSS AR24

PLACE THESE GAP CLOSE TO APU.

EXP A\_RXP[0..15] >> EXP\_A\_RXP[0..15] 14  
EXP A\_RXN[0..15] >> EXP\_A\_RXN[0..15] 14  
EXP A\_TXP[0..15] >> EXP\_A\_TXP[0..15] 14  
EXP A\_TXN[0..15] >> EXP\_A\_TXN[0..15] 14

28 ML\_IP >> AF5  
28 ML\_IN >> AF6  
14 PCIE1\_IP >> AF8  
14 PCIE1\_IN >> AF9

AE7  
AE8  
AD5  
AD6

10 A\_RX0P >> AJ8  
10 A\_RX0N >> AJ7  
10 A\_RX1P >> AH6  
10 A\_RX1N >> AH5  
10 A\_RX2P >> AH9  
10 A\_RX2N >> AH8  
10 A\_RX3P >> AG8  
10 A\_RX3N >> AG7

APU\_VDD12 AR25 196/4/1 P\_ZDD AJ2

Within 1500mil from APU

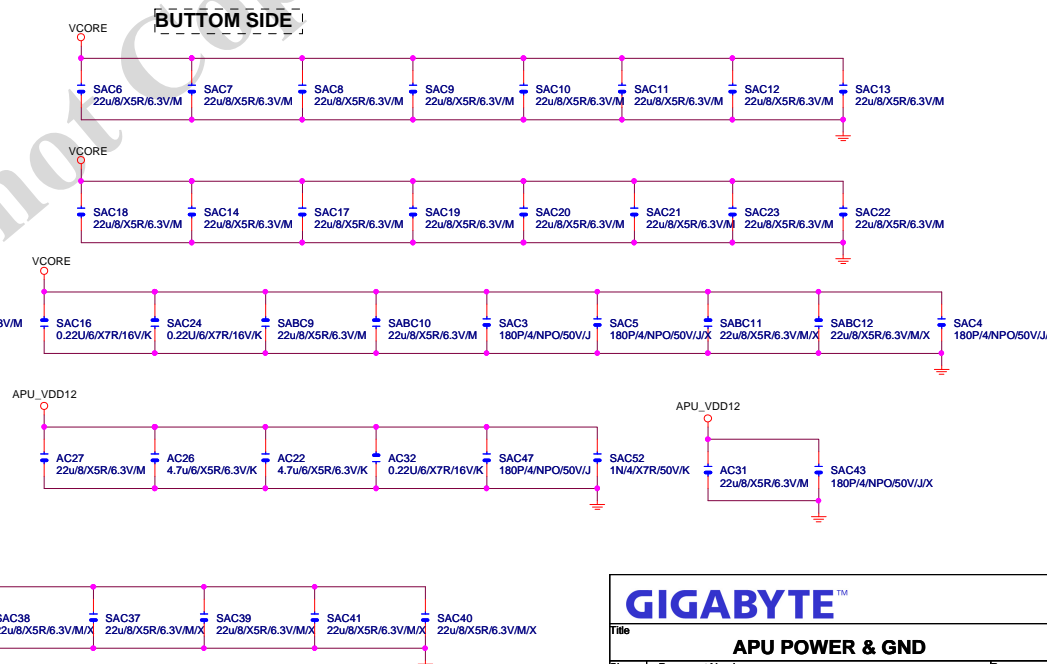
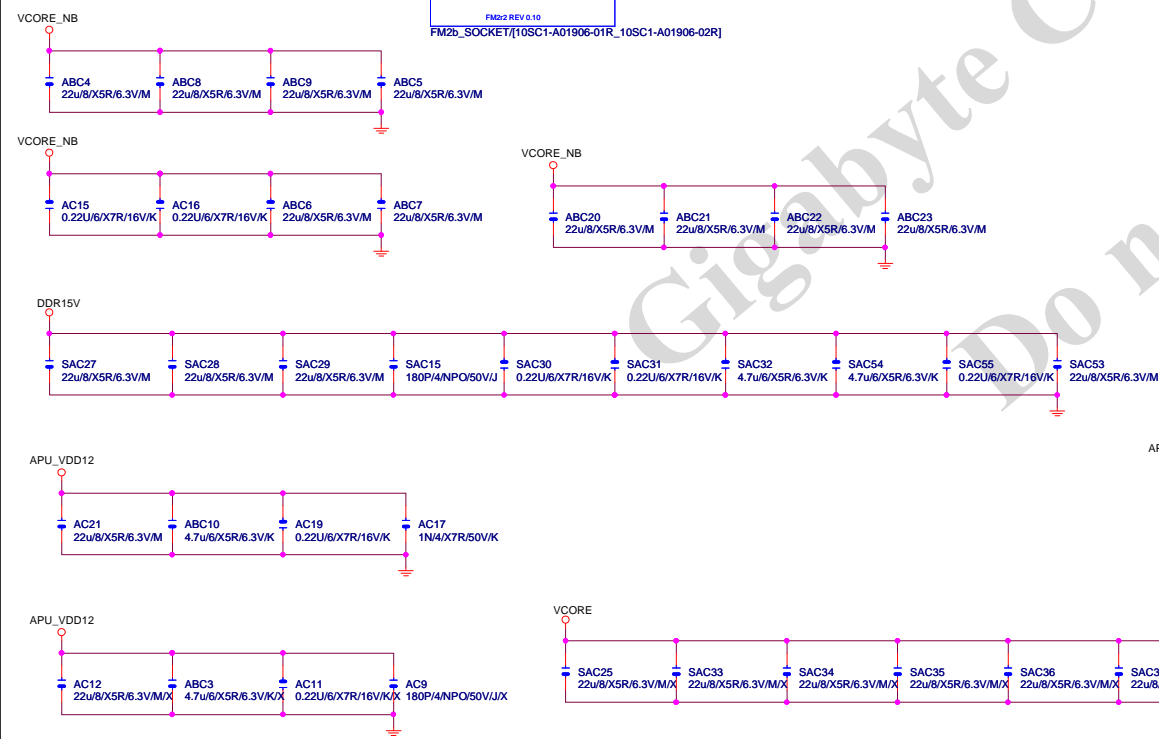
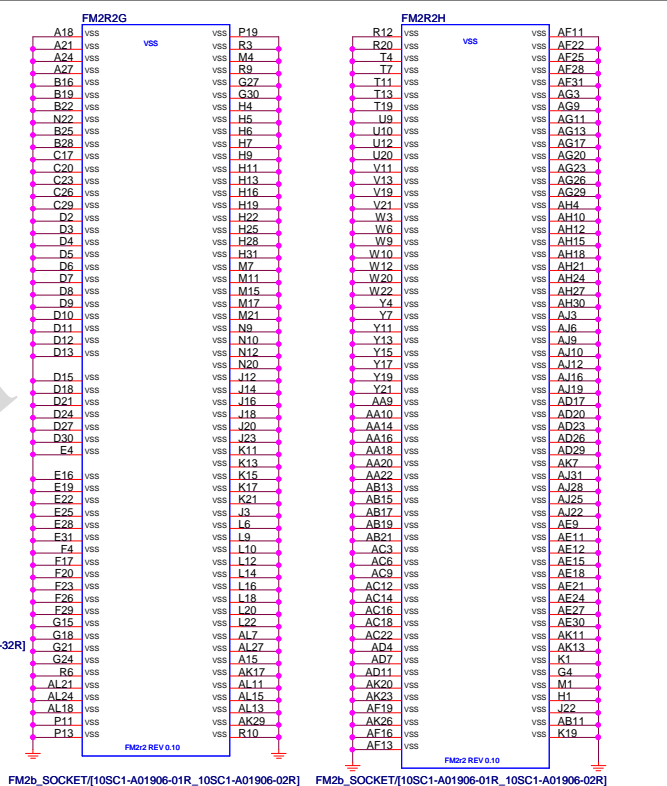
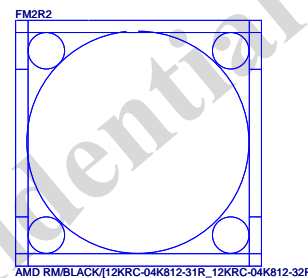
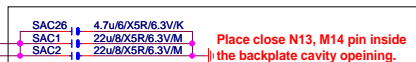
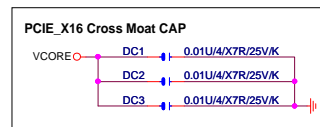
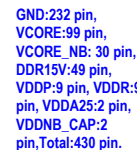
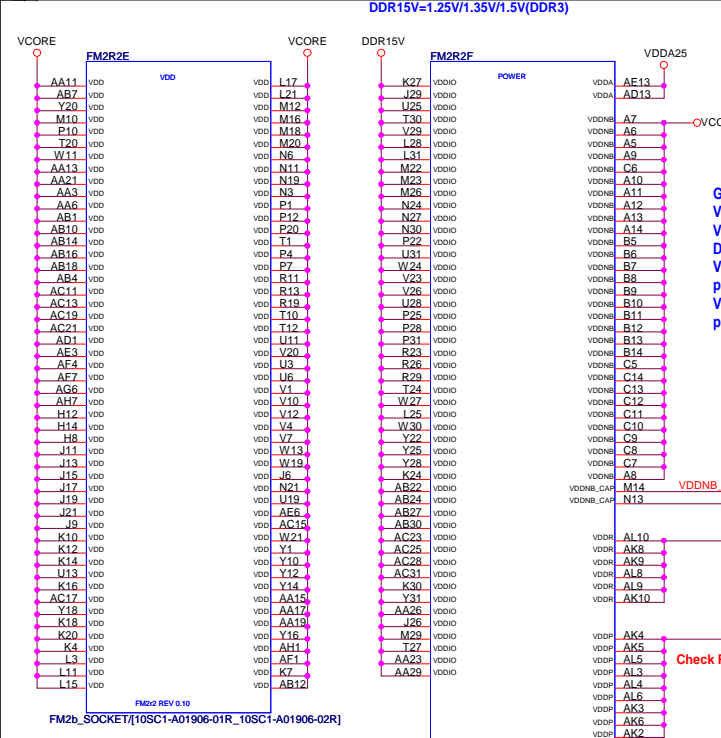
Within 1500mil from APU

GIGABYTE™

Title APU GFX, GPP, UMI I/F

Size Custom Document Number GA-F2A88XM-D3H Rev 3.1

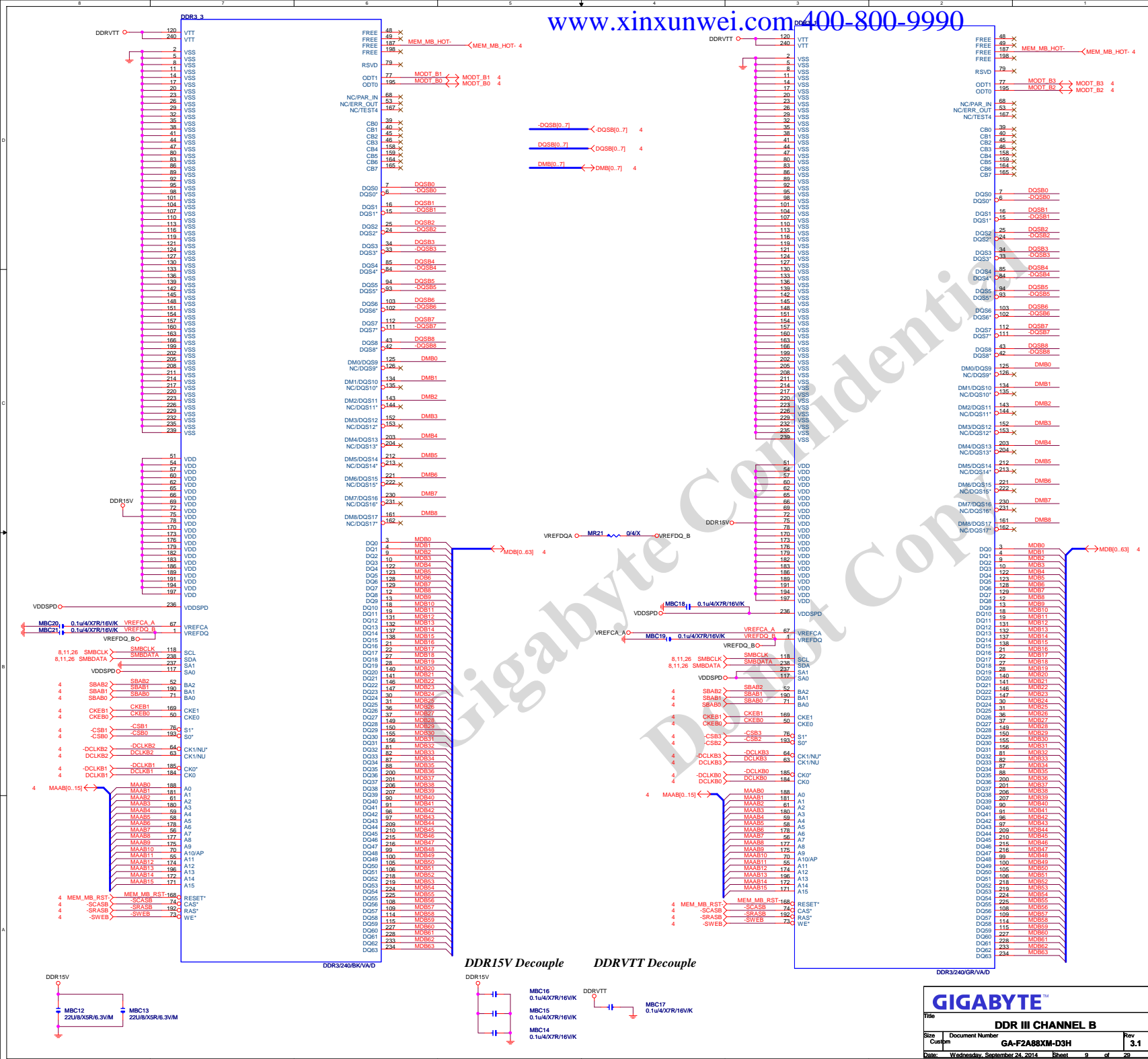
Date: Wednesday, September 24, 2014 Sheet 6 of 29











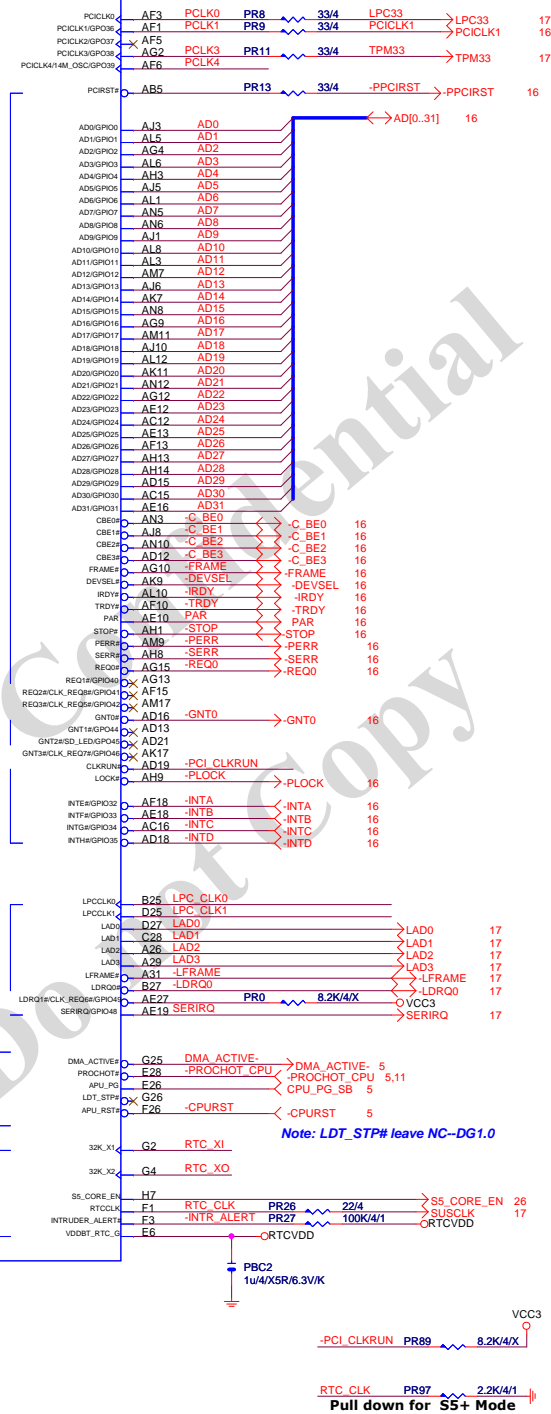
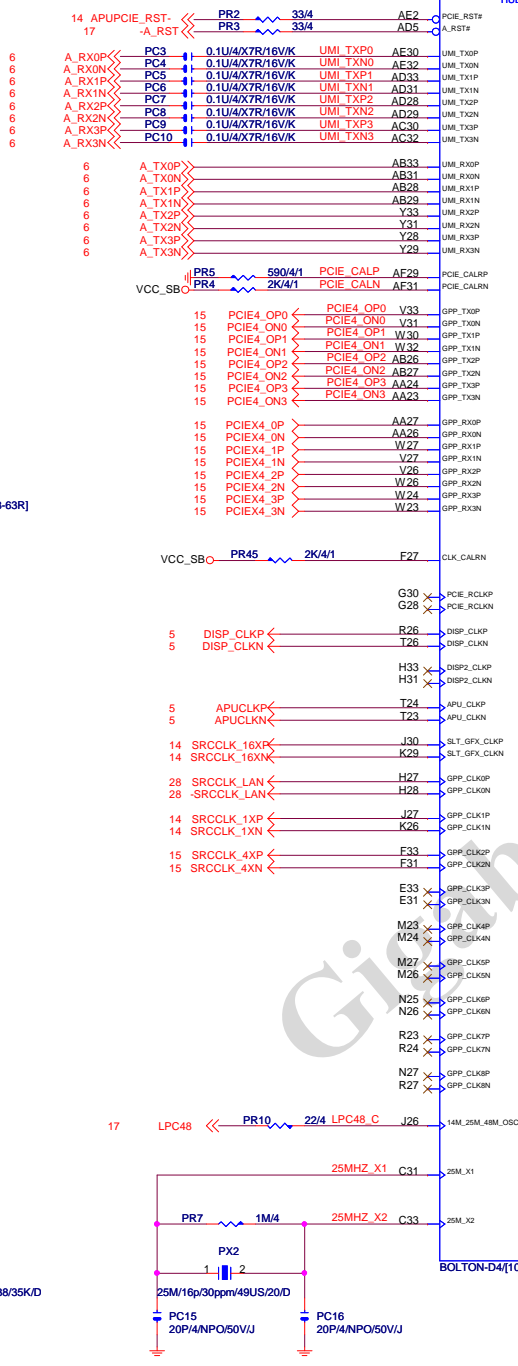


PLACE THESE PCIE AC COUPLING  
CAPS CLOSE TO SB850

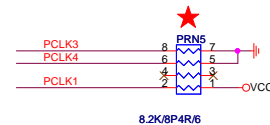
**S.B HEATSINK**

1 SB\_HS

SB\_HS[12SP2-S04208-61R\_12SP2-S04208-62R\_12SP2-S04208-63R]



Low: Force PCIE GEN1, Up: Allow PCIE GEN2



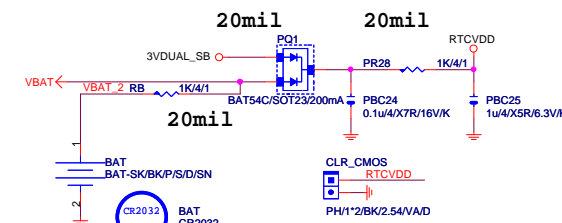
	PCLK3
PULL HIGH	USE DEBUG STRAPS
PULL LOW	IGNORE DEBUG STRAPS DEFAULT



**CLKGEN Mode:** Only for integrated clock mode.



	LPC_CLK0	LPC_CLK1
HL	IMC	CLKGEN
HH	ENABLED	ENABLED
	AOD Extreme	
LL	IMC	CLKGEN
LV	DISABLED	DISABLED
	DEFAULT	DEFAULT



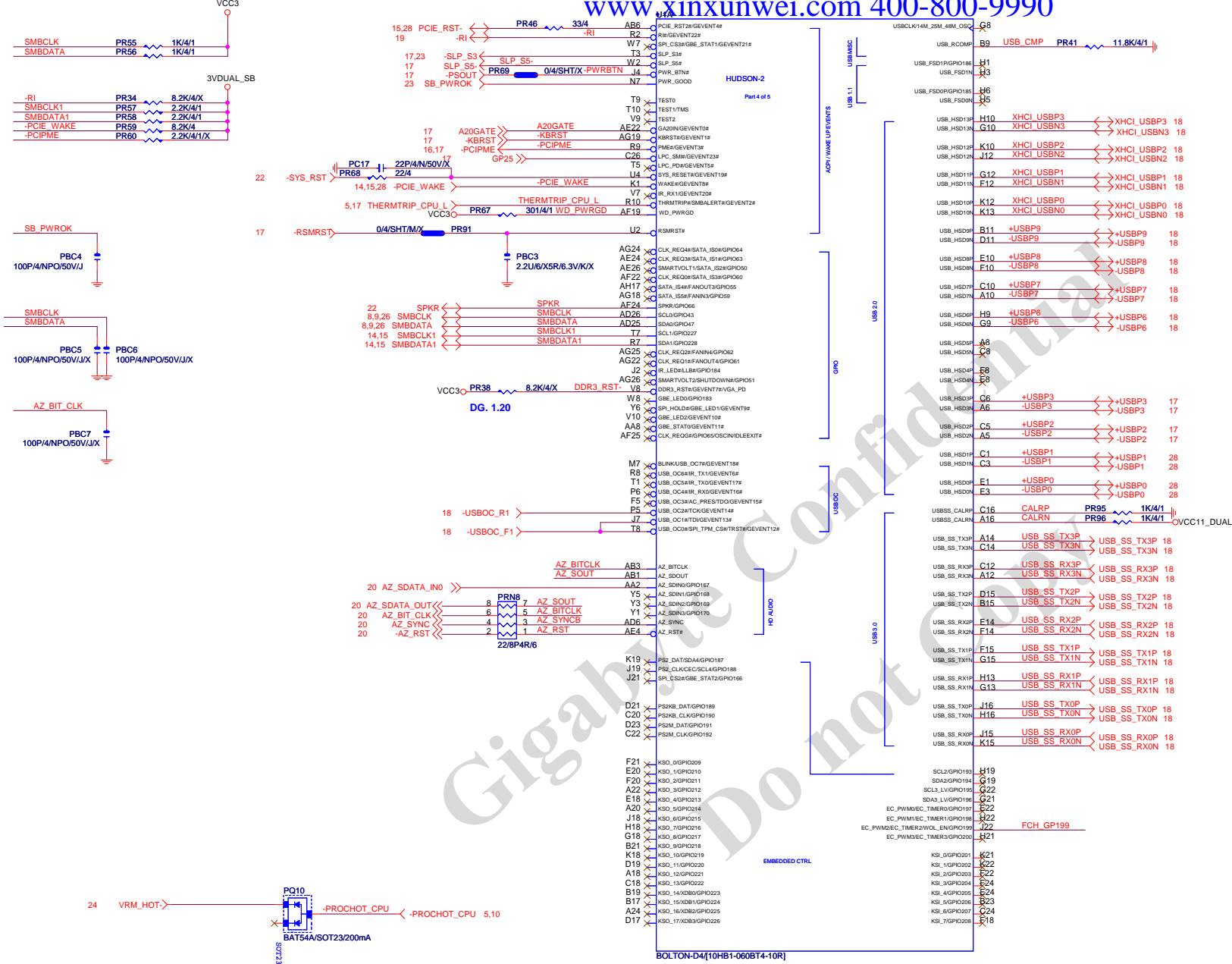
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

**GIGABYTE**

Title	HUDSON D4 PCIE/PCI/CPU/LPC
-------	----------------------------

Size	Document Number	Rev
Custom	GA-F2A88XM-D3H	3.1



USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR\_GD signals  
can be used for power-up sequencer

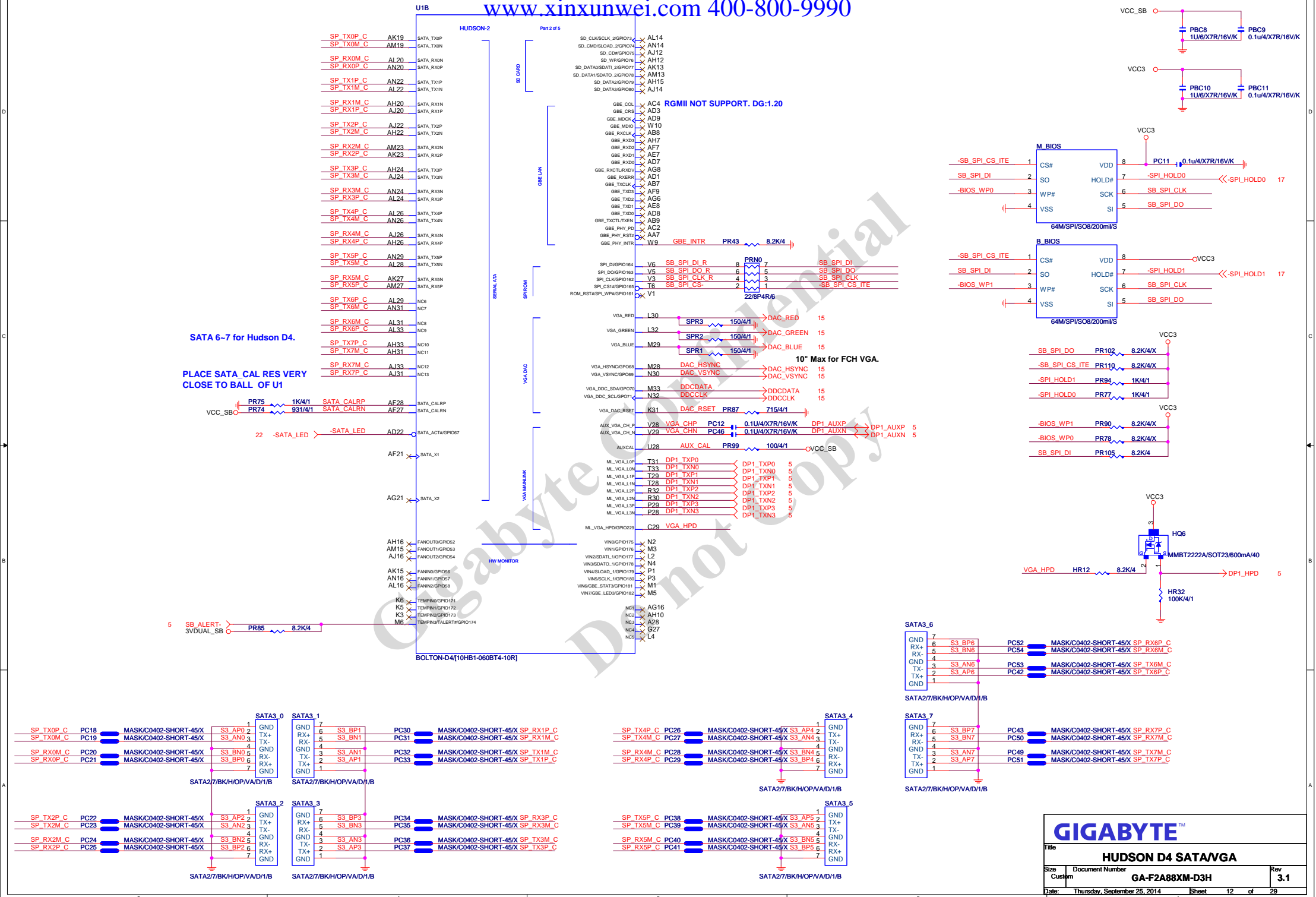
FCH\_GP199 PR62 2.2K/4/1

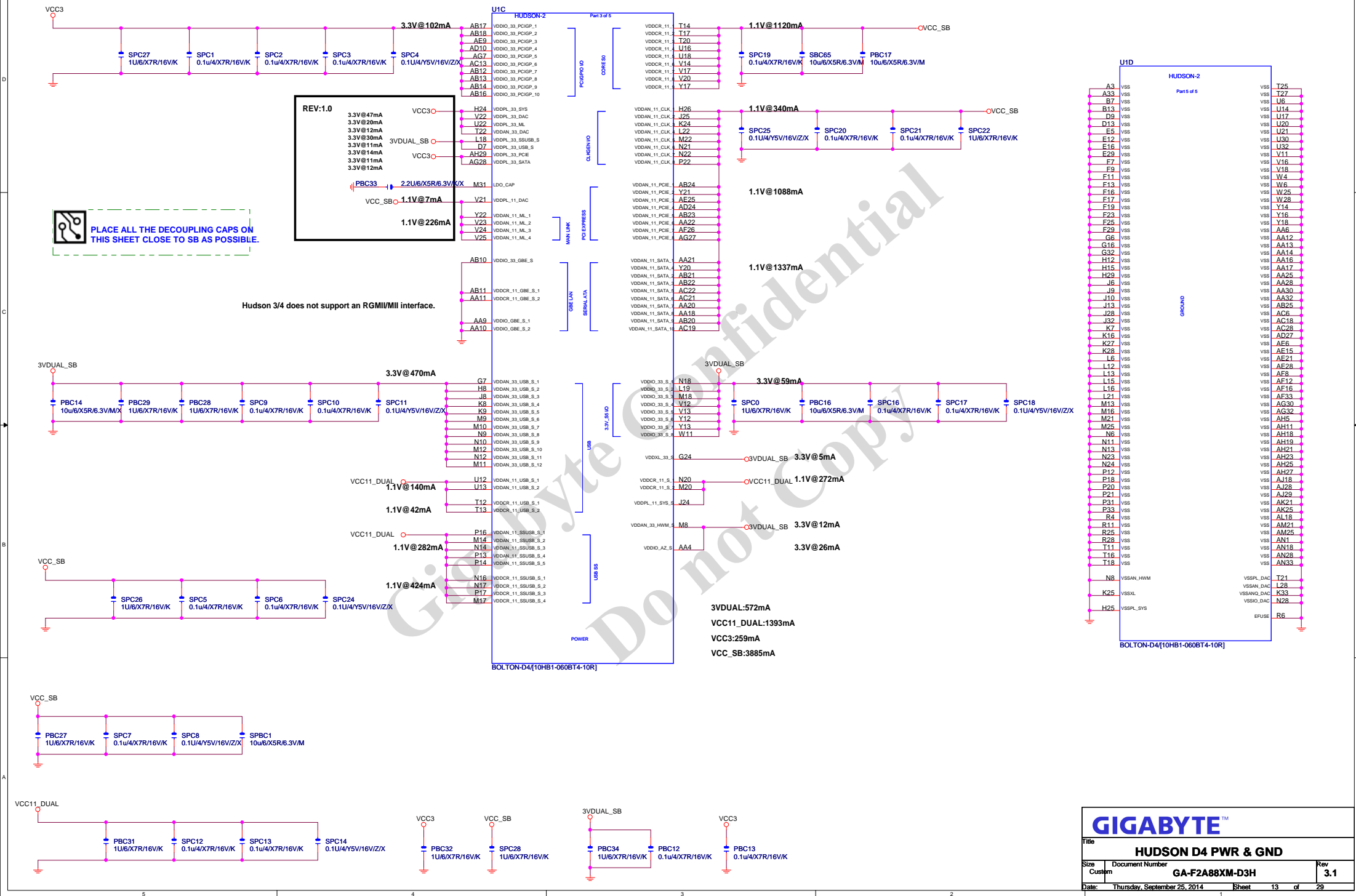
**FCH\_GP199**

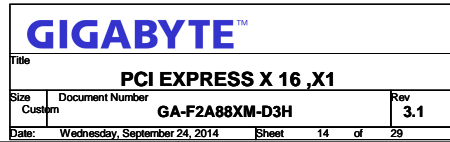
ROM TYPE:

H = LPC ROM

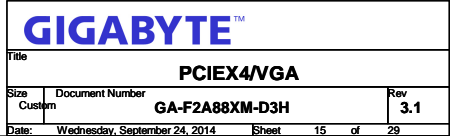
L = SPI ROM <Default>



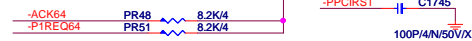
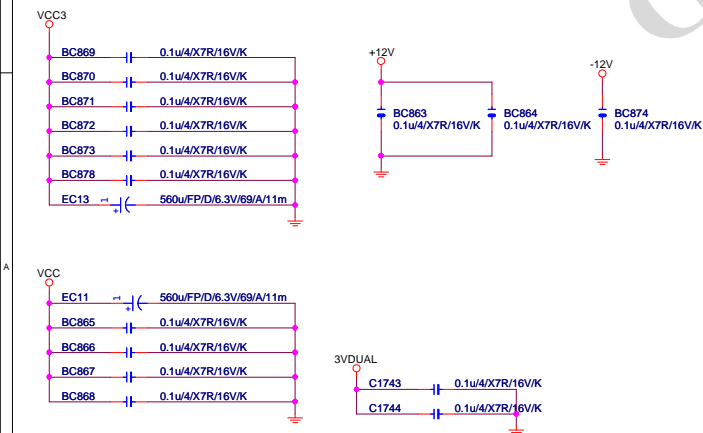


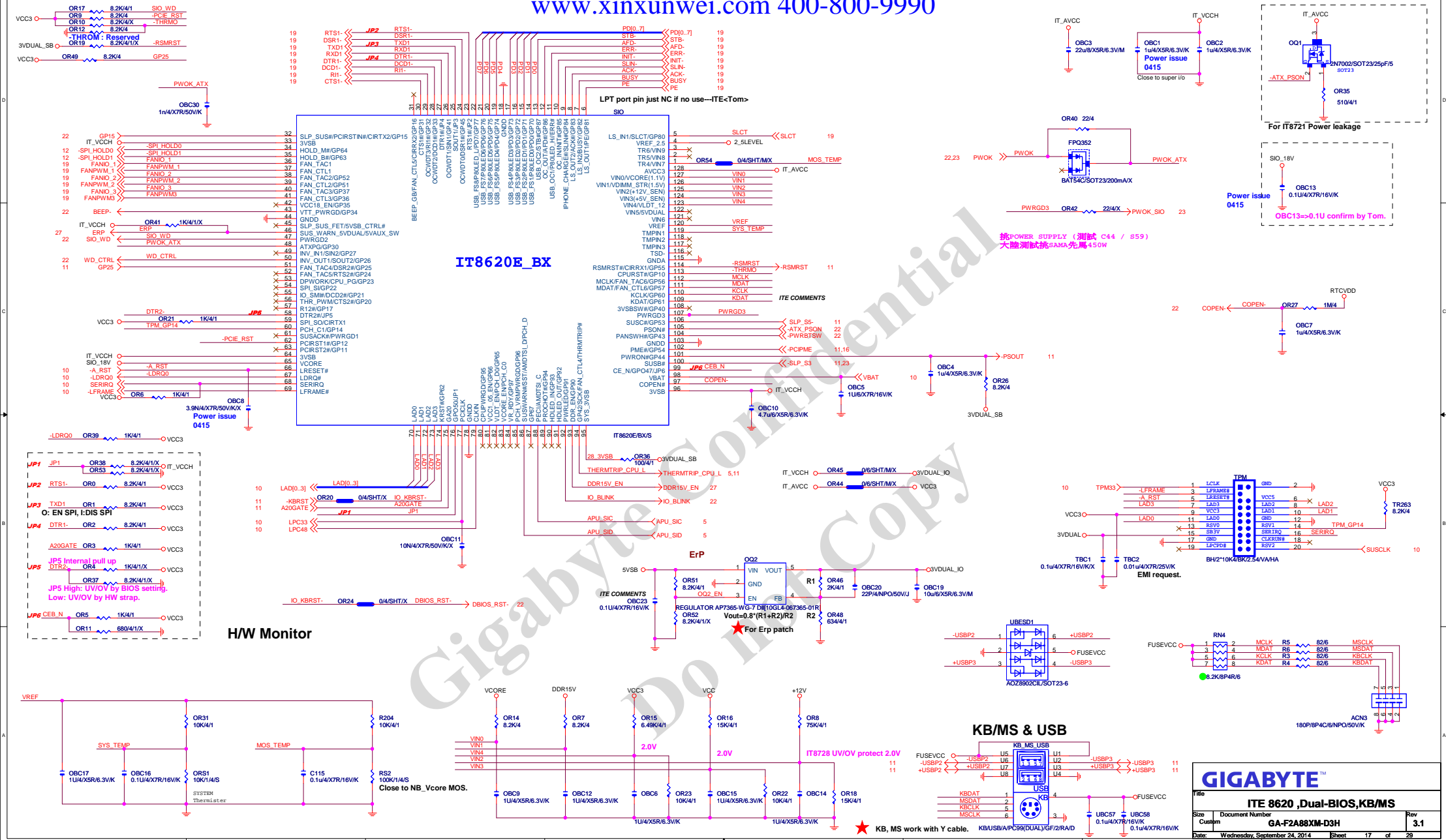


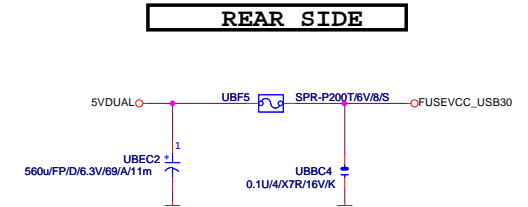
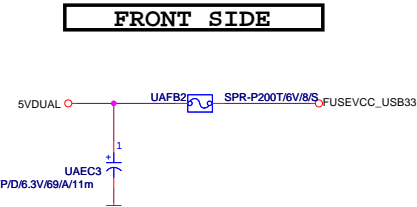
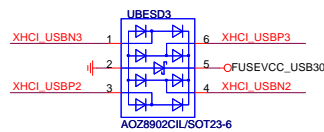
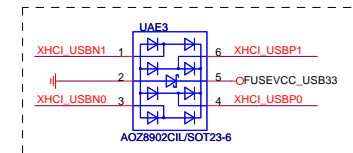
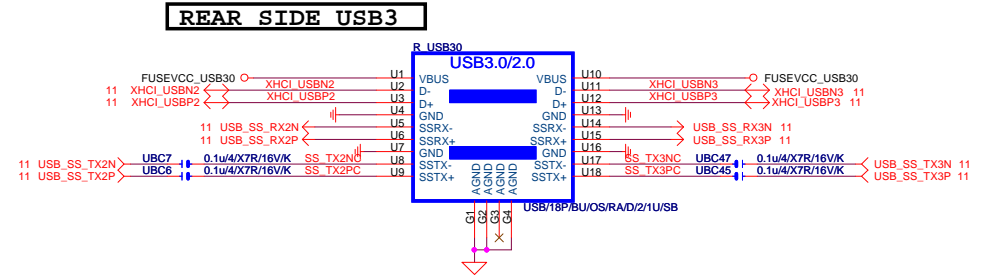
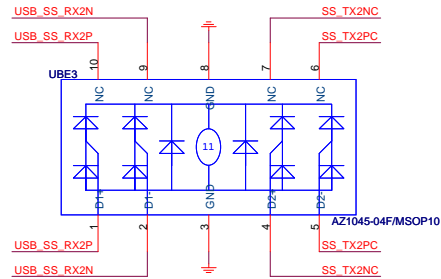
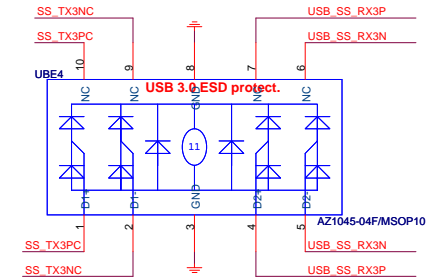
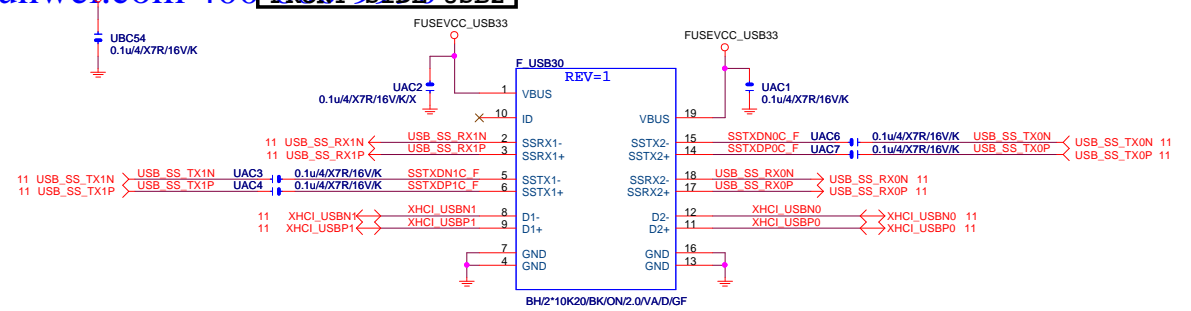
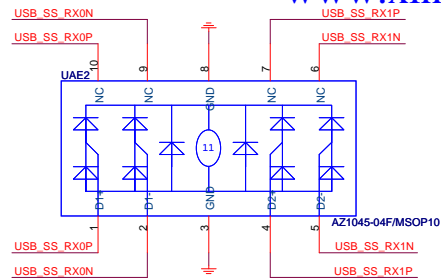
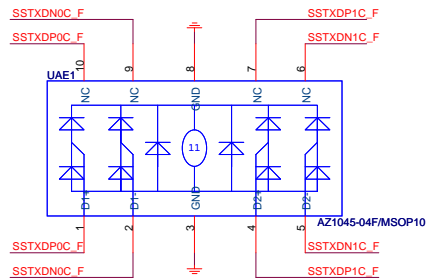




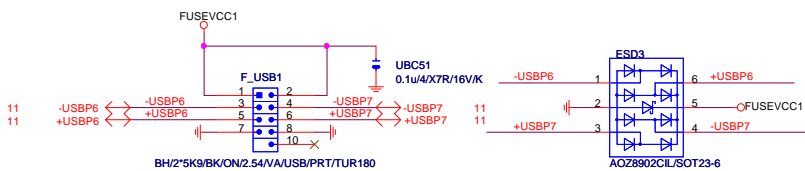




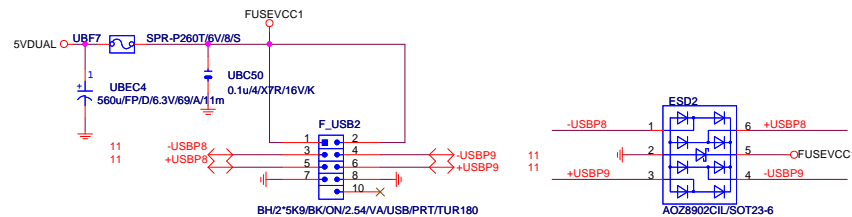




## FRONT SIDE USB1

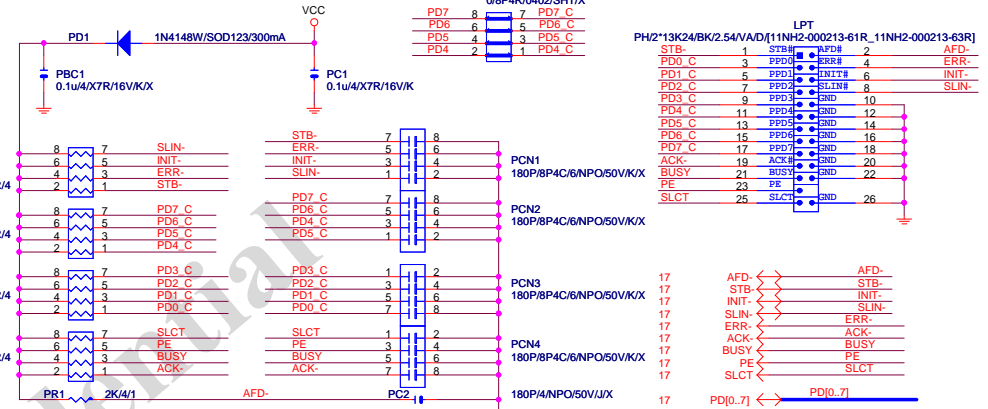
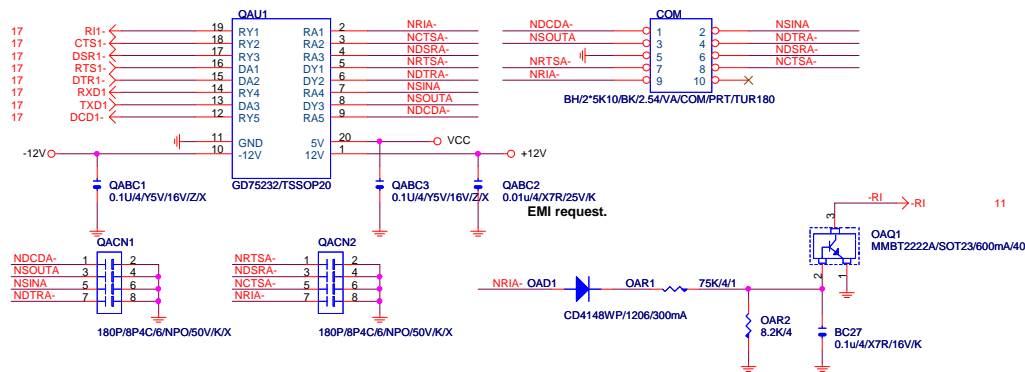


## FRONT SIDE USB2



COM

LPT



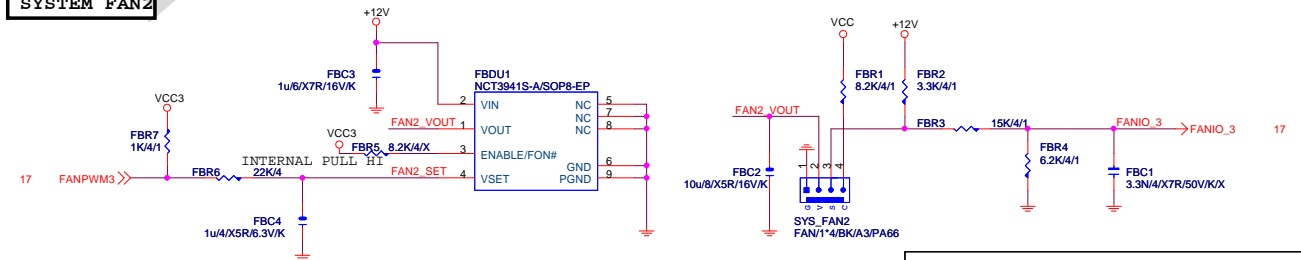
## CPU SMART FAN

## SYSTEM FAN1

## Linear SYS\_FAN

Enable Function (NCT3941S)  
Full Turn On Function (NCT3941S-A)

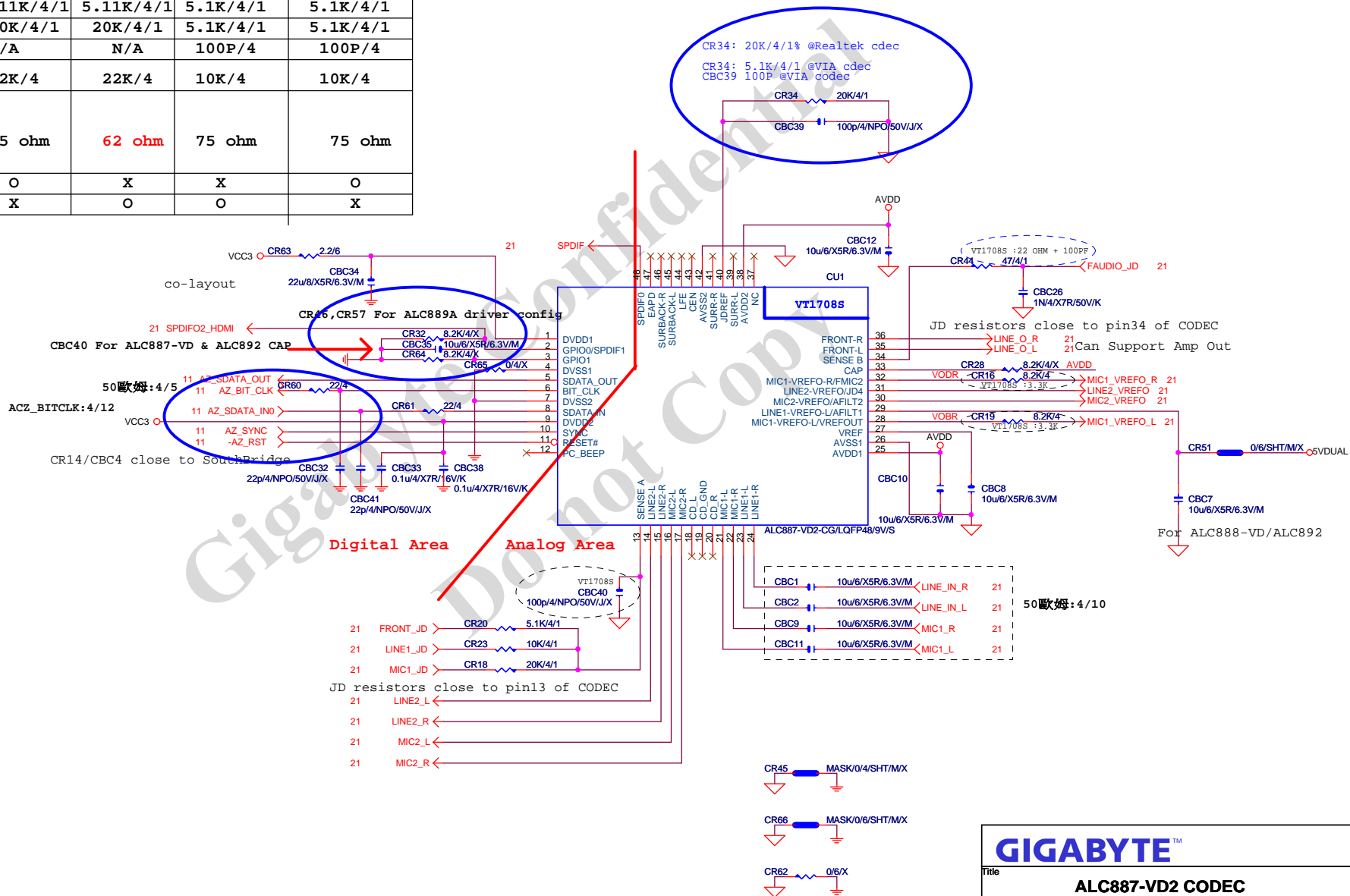
## SYSTEM FAN2



GIGABYTE™

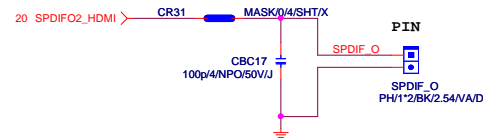
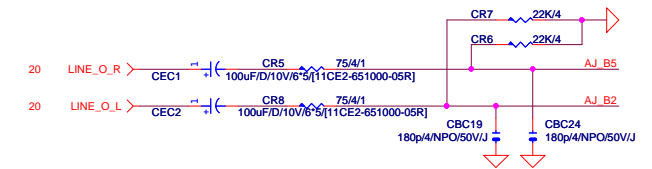
Title		
CPU & SYS FAN COM, LPT, MOSFET HOT		
Size	Document Number	Rev
Custom	GA-F2A88XM-D3H	3.1
Date:	Wednesday, September 24, 2014	Sheet 19 of 29

	ALC887-VD2	ALC889	VT1708S	VT1708SCE
CR65	X	O	O	X
CR64	X	X	X	O
CR44/CBC6	47ohm+1nF	47ohm+1nF	22ohm+100P	22ohm+100P
CR34	20K/1%	20K/1%	5.1K/1%	5.1K/1%
CR31	O	O	O	O
CR30	X	X	X	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R	22uF/X5R
CR20	5.11K/4/1	5.11K/4/1	5.1K/4/1	5.1K/4/1
CR34	20K/4/1	20K/4/1	5.1K/4/1	5.1K/4/1
CBC39/CBC40	N/A	N/A	100P/4	100P/4
CR6/CR7/CR54/CR58	22K/4	22K/4	10K/4	10K/4
CR5/CR8/CR1/CR14/ CR17/CR22/CR13/CR11/ CR57/CR53	75 ohm	62 ohm	75 ohm	75 ohm
CR51/CD1/CBC7	O	X	X	O
CD2/CD3/CQ3/CQ5	X	O	O	X



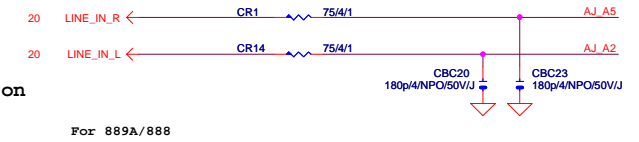
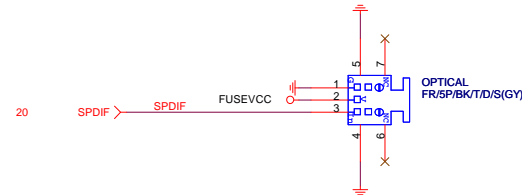
GIGABYTE™

Title	ALC887-VD2 CODEC		
Size	Document Number	Rev	3.1
Custom	GA-F2A88XM-D3H		
Date:	Thursday, September 25, 2014	Sheet	20 of 29

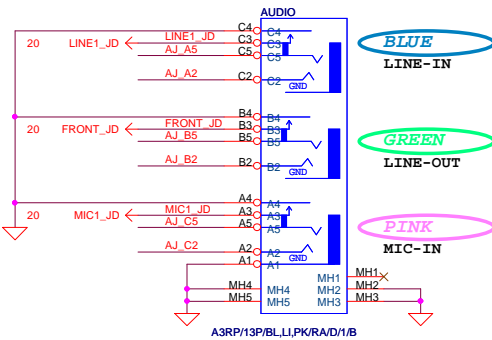
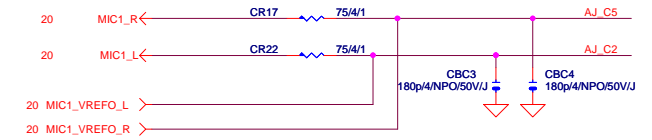
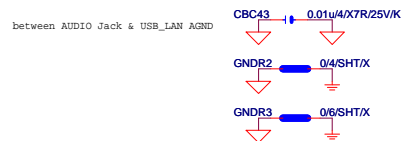
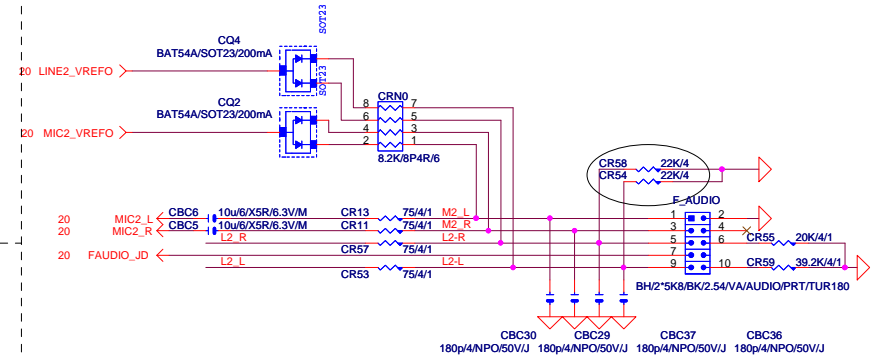
**SPDIF\_OUT****LINE-OUT****LINE-IN**

Verify MIC function  
in LINE-in

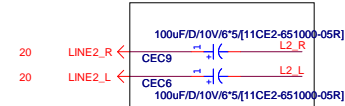
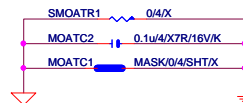
Only reserved for ALC888

**2 type Connector Co-lay****1.0/1.1 Selection**

	HDMI_SPDIF	OPTICAL	CR40
Rev: 1.0	V	X	V
Rev: 1.1	HDMI	V	X

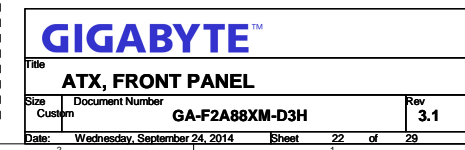
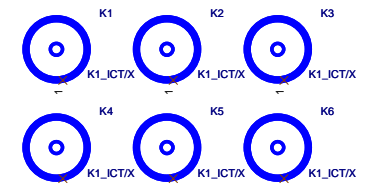
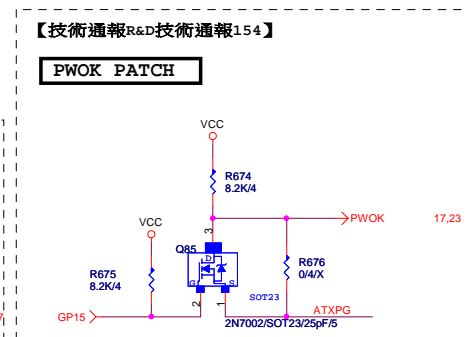
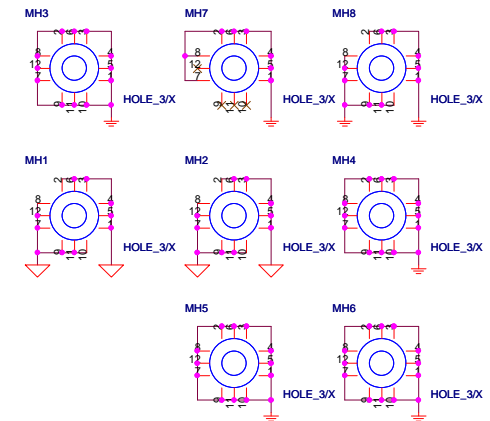
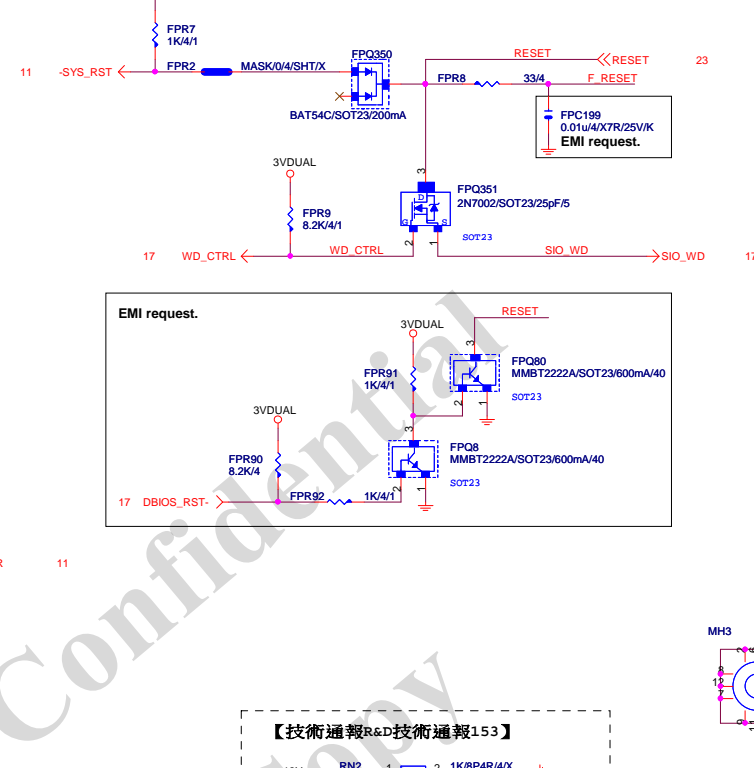
**HD Audio Jack****MIC-IN****AZALIA FRONT PANEL**

F\_AUDIO  
Codec --> Audio Jack  
Near Audio Jack Left  
Under Codec body

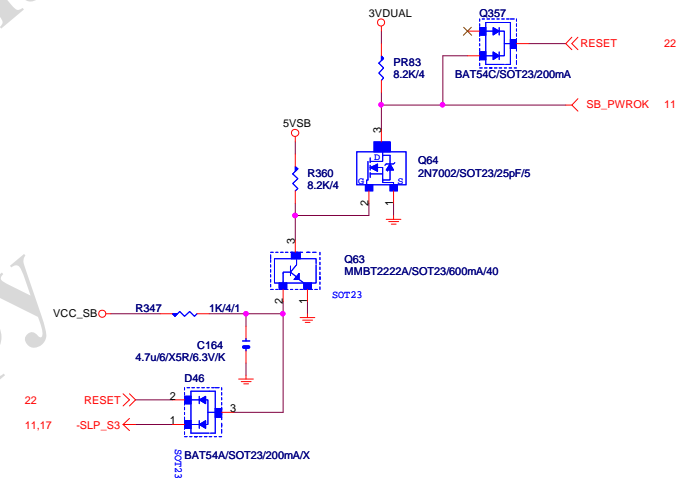
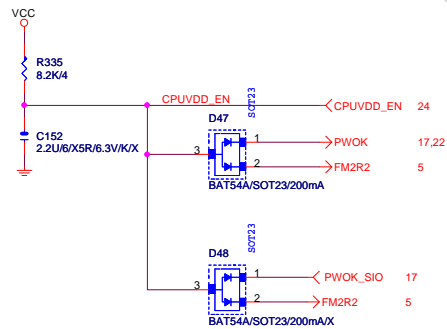
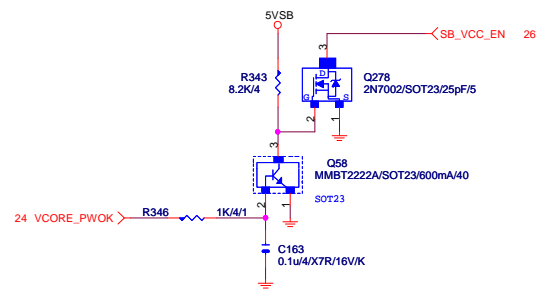


**GIGABYTE**™

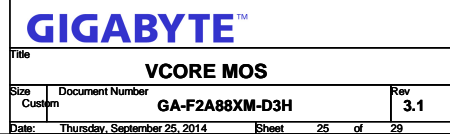
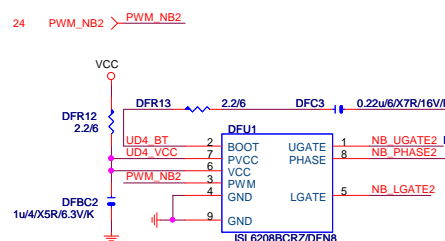
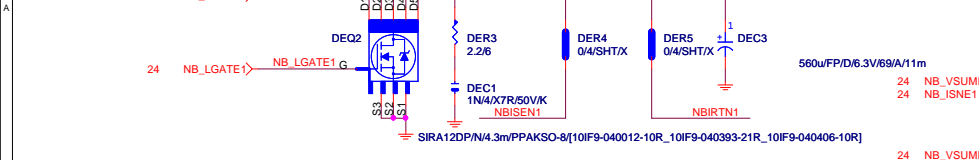
Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	GA-F2A88XM-D3H	3.1
Date:	Monday, September 29, 2014	Sheet 21 of 29



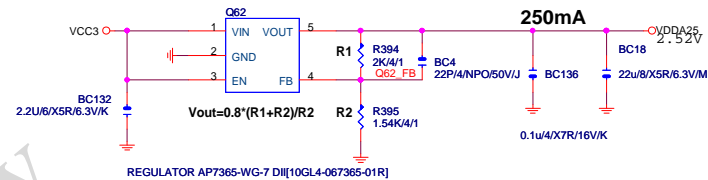
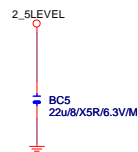








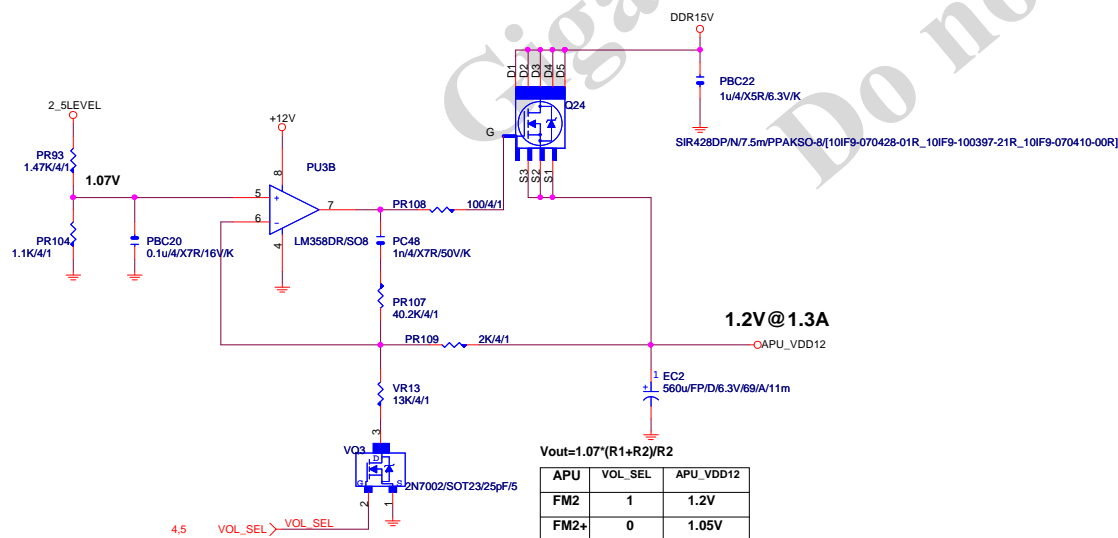
## VCC\_SB



APU	VOL_SEL	VDDA25
FM2	1	2.5V
FM2+	0	1.8V

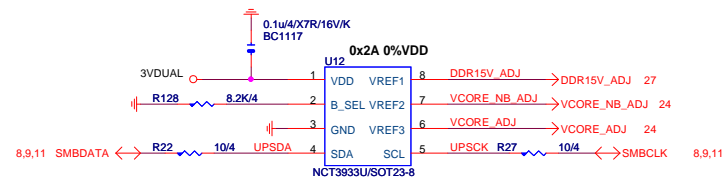
4.5 VOL\_SEL VOL\_SEL

## APU\_VDDP



APU	VOL_SEL	APU_VDD12
FM2	1	1.2V
FM2+	0	1.05V

4.5 VOL\_SEL VOL\_SEL



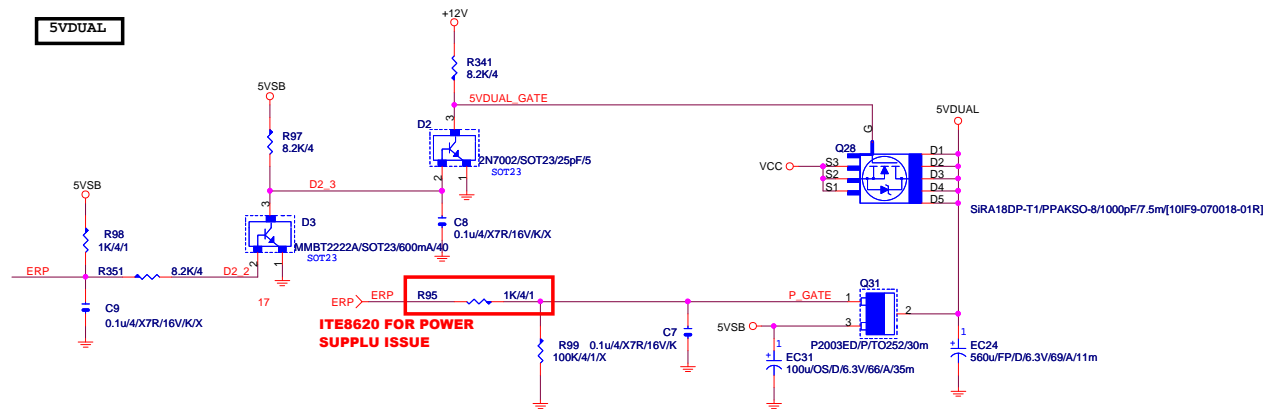
GIGABYTE™

Title SB PWR,VDDA25,VCC11DUAL

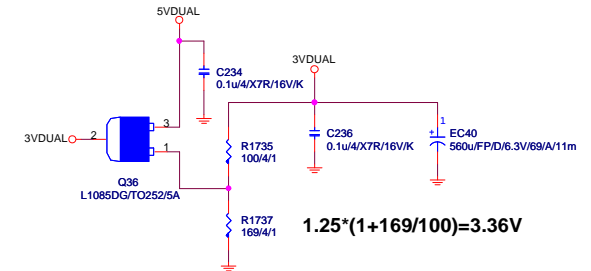
Size Custom Document Number GA-F2A88XM-D3H Rev 3.1

Date: Thursday, September 25, 2014 Sheet 26 of 29

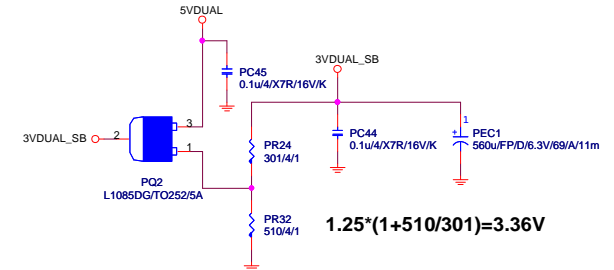
## 5VDUAL



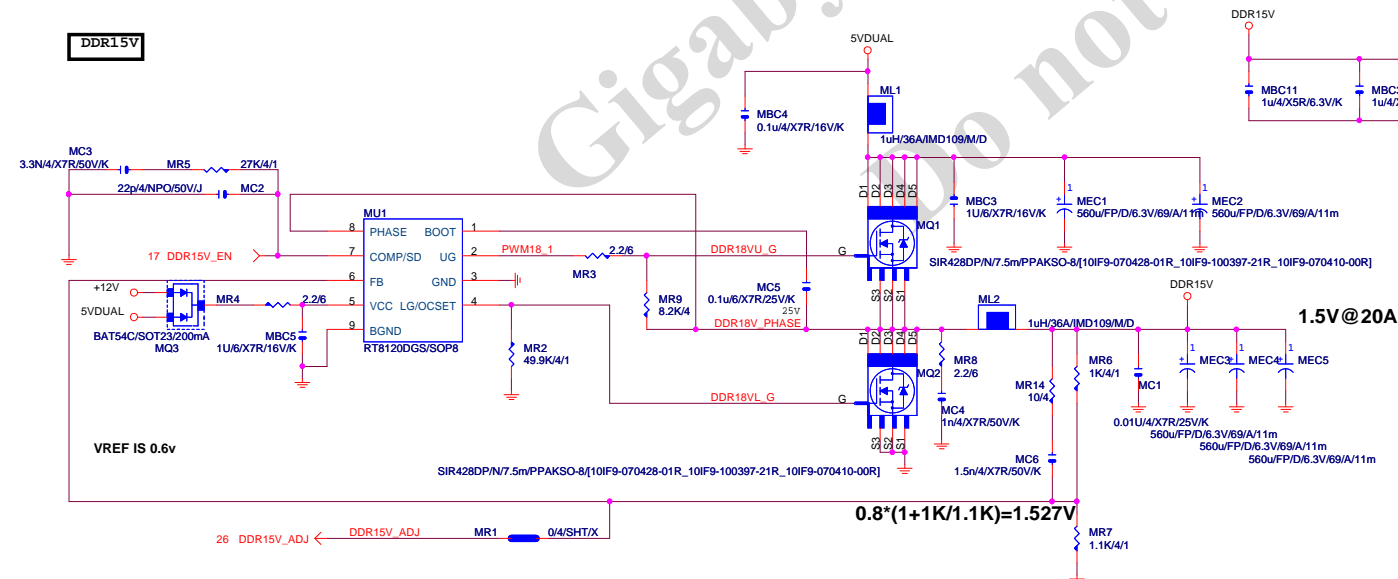
## 3VDUAL



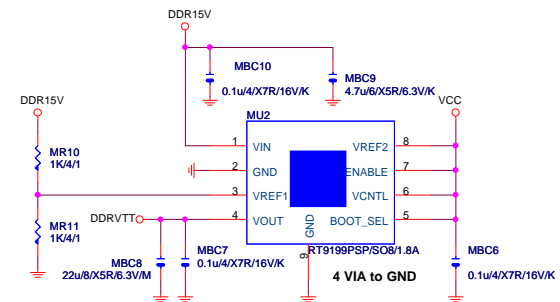
## 3VDUAL\_SB



## DDR15V



## DDRVTT



GIGABYTE™

Title		
DDR PWR, 5VDUAL, ERP		
Size	Document Number	Rev
Custom	GA-F2A88XM-D3H	3.1
Date:	Friday, September 26, 2014	Sheet 27 of 29



